Electronics/Electrical

Schottky Barrier Modulation for Next-Gen MOS Devices
Technology Domain: Semiconductors
Patent Application Number: 202441030109
Status (Patent/TRL): Patent Pending / TRL 3
Technology Summary: This invention provides novel methods to reduce Schottky barrier height and contact resistance in advanced Metal-Oxide-Semiconductor (MOS) transistors, addressing a critical challenge in miniaturized semiconductor devices. The key technical solution involves interface engineering by integrating ultra-thin (5-10 Angstrom) cap layers of specific semiconductor materials between the main semiconductor substrate (SiGe or pure Si) and the contact metal (e.g., TiSiGe, TiSi2, TiGe2). For n-type devices, cap Germanium (Ge) layers are used, while for p-type devices, cap Silicon (Si) layers are employed. A crucial inventive feature is forming a sufficiently thick (20-25 Angstrom) SiGe or Si layer on top of these cap layers to prevent their consumption during subsequent high-temperature thermal processes like silicidation or germanidation, thus preserving the cap layer's functionality. The results demonstrate a significant reduction in both n-type and p-type Schottky barrier heights and corresponding contact resistance, enhancing device performance. This technology is highly useful for optimizing various advanced semiconductor architectures, including FinFETs, Gate All Around FETs, FDSOI, ETSOI, and planar CMOS, enabling further miniaturization and improved efficiency in next-generation electronic devices.